Remarks

Claim 16 has been amended. No new claims have been added. Claims 16-19 are pending. Claims 1-15 and 20-23 were withdrawn.

Examination and reconsideration of the claims as amended is requested.

Support for the amendment to claim 16 is found in the specification as filed, for example, in Figures 1A and 1B, and in the originally filed claims.

Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a) as not showing a feature recited in claim 16. It is submitted that the amendment to claim 16 overcomes this objection. Claim 16 now recites "the bumped side of the integrated circuit chip". Figures 1A and 1B clearly show this feature (IC chip 20) as described on 11, lines 4-10 of the present application. Thus, it is believed that this objection should be withdrawn.

§ 112 Rejection

Claims 16-19 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Examiner states that in claim 16, the recitation of "the bumped side of the circuit substrate" is unclear as to whether this bumped side (of the circuit substrate) is similar to or different from "a bumped side having a passivation surface". It is further asserted that in claim 16, the limitation "the circuit substrate" has no antecedent basis. Finally, claims 17-19 are rejected since each includes the limitations of independent claim 16.

It is believed all these rejections have been addressed by the amendment to claim 16 and claims 16-19 are now allowable.

§ 102 Rejections

Claims 16-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hideshima et al. (U.S. Patent No. 5,143,865) and Akram et al. (U.S.Patent No. 5,956,605) separately.

The Examiner asserts that Hideshima discloses (specifically in Figure 2) an integrated circuit chip (10) comprising: a bumped side having a passivation surface (e.g., the passivation layer 14) on which a plurality of conductive bumps (18) are disposed; layer of adhesive (17) covering the bumped side of the circuit substrate, the adhesive layer having a primary surface that is substantially parallel to the passivation surface, and the conductive bumps (18) having exposed contact regions that are not covered by the adhesive (17), wherein the exposed contact regions of the conductive bumps have a rounded profile.

The Examiner's argument is founded upon the erroneous characterization of Hideshima layer 17 as an adhesive. In fact, Hideshima expressly describes layer 17 as an "insulation film (SiN film)" (col. 5, line 16). The Examiner has not shown that SiN is an adhesive. Further, it is believed that the Examiner cannot show this. For example, SiN is understood in the art as silicon nitride, a ceramic coating, which is actually a passivation layer material. Thus, the Examiner's argument fails to describe the adhesive layer as required in the present invention and Hideshima does not anticipate the claims of the present invention.

The Examiner's argument regarding claim 17 also lacks the required adhesive layer. Thus, the Examiner's argument fails to meet the requirements for anticipation and this rejection should be withdrawn.

The Examiner's argument also asserts that Akram (specifically Figure 10) teaches a structure identical to Hideshima's device structure, and concludes that Akram also anticipates the claimed invention for the same reasons given with respect to Hideshima.

Again, the Examiner's argument is founded upon an erroneous characterization. Figure 10 in Akram discloses a silicon nitride layer 22 (col. 8, lines 36-38). As with Hideshima, the Examiner's argument characterizes a layer of silicon nitride as an adhesive layer. As taught by the Akram reference itself (e.g., col. 2, lines 31-35), silicon nitride is a passivation layer material. Thus, the Examiner's argument again fails to describe the adhesive layer as required in the present invention and Akram does not anticipate the claims of the present invention.

In summary, the rejection of claims 16-19 under 35 U.S.C. § 102(b) as being anticipated by either Hideshima or Akram should be withdrawn.

In view of the foregoing, Applicants believe that all outstanding grounds of rejection have been overcome by this response and that the presently pending claims are hereby placed in

condition for allowance. If a teleconference would be helpful in resolving any outstanding matters in the present application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,

27 Jan 2003
Date

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Version with Changes Marked

In the Specification

On pages 11-12, please amend the following paragraph starting on page 11 line 26 and ending on page 12 line 9:

To ensure a better electrical connection with a substrate, it is preferred to at least partially remove the adhesive protuberances 28 that cover the bumps 24. As shown in Fig. 1B, an abrasion process is employed to remove the adhesive material located on top of the bumps 24 exposing the conductive bumps 24 for better electrical connection with a packaging substrate. In the abrasion process, an abrasive material 32 such as sandpaper, micro abrasive, abrasive pads available from 3M Company, St. Paul, MN under the trade designation [Scotch Bright] Scotch Brite, a cloth, a scraping blade or a coating knife is brought in contact with the adhesive protuberances 28 that cover the bumps 24 such that the bumps 24 are exposed for electrical conduction. Because the protuberances project above the average adhesive height on the chip 20, such protuberances become pressure focal points that receive the most abrasion or cutting. Fig. 1C shows the chip 20 after the bumps have been exposed via abrasion. Once the bumps have been exposed, a film, tape or other type of protective cover may be applied to the chip 20 to protect the adhesive 26 and the exposed bumps 24.